We claim:

1. In an integrated circuit chip including first and second supply potentials, a method of making a programmable memory cell for storing a value, the method comprising:

forming a plurality of metal layers separated by a plurality of via layers;

forming a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias in the plurality of via layers;

forming a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias in the plurality of via layers;

coupling together said first and second metal interconnect structures at a top metal layer prior to programming;

coupling one of the first and second supply potentials to at least one of said first and second metal interconnect structures to form an output; and

altering at least one of the plurality of metal layers to thereby program the output.

2. The method of claim 1, further comprising forming multiples of the first and second metal interconnect structures and coupling together the first and second metal interconnect structures to form a plurality of programmable cycles for the memory cell, wherein each half cycle is programmable at least once.

3. The method of claim 2, further comprising forming a one cycle ladder structure that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer.

4. The method of claim 3, further comprising forming the ladder structure in a shape of a cube.

5. The method of claim 4, further comprising forming the first and second supply potentials as two buses located in a central region of said cube-shaped structure and so as to be accessible at each of the metal layers.

6. The method of claim 4, further comprising forming the ladder structure in a shape of a spiral.

7. The method of claim 6, further comprising forming the first and second supply potentials as buses accessible at each of the metal layers.

8. The method of claim 1, further comprising altering any one of the plurality of metal layers to thereby reprogram at least one of the first and second metal interconnect structures.

9. The method of claim 8, further comprising repeating the reprogramming.

10. The method of claim 1, further comprising altering any one of a plurality of via layers to thereby reprogram at least one of first and second metal interconnect structures.

11. The method of claim 10, further comprising repeating the reprogramming.

12. The method of claim 1, further comprising altering any one of the plurality of metal layers or any one of a plurality of via layers to thereby reprogram the first and second metal interconnect structures.

13. The method of claim 12, further comprising repeating the reprogramming.

14. In an integrated circuit chip including first and second supply potentials, a method of making a programmable memory cell for storing a value, the method comprising:

forming a plurality of metal layers separated by a plurality of via layers;

forming a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias in the plurality of via layers;

forming a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias in the plurality of via layers;

coupling together said first and second metal interconnect structures at a top metal layer prior to programming;

coupling the first supply potential to the first interconnect structure and the and second supply potential to the second interconnect structure to form two outputs; and

altering at least one of the plurality of metal layers to thereby program at least one of the outputs.

15. The method of claim 14, further comprising coupling one of the first and second metal interconnect structures to the first supply potential at a bottom metal layer and coupling the other of the first and second metal interconnect structures to the second supply potential at the bottom metal layer.

16. The method of claim 15, further comprising arranged the first and second metal interconnect structures to from a ladder structure.

17. The method of claim 15, further comprising arranged the first and second metal interconnect structures to from an offset ladder structure.

18. The method of claim 15, further comprising arranged the first and second metal interconnect structures to from a stacked structure.

19. The method of claim 18, further comprising forming the stacked structure using first and second alternating metal interconnect patterns.

20. The method of claim 19, further comprising:

forming the first alternating metal interconnect pattern using first and second interspersed metal traces, and

forming the second alternating metal interconnect pattern using third and fourth interspersed metal traces, and

forming the third and fourth interspersed metal traces as a mirror image of first and second interspersed metal traces.

21. The method of claim 20, further comprising interconnecting the first and third interspersed metal traces using the first plurality of vias and interconnecting ones of the second and fourth interspersed metal traces using the second plurality of vias.

22. The method of claim 21, wherein the memory cell is programmed at any metal layer by:

forming an open circuit in each of said first and second interspersed metal traces of that layer thereby splitting each metal trace into two portions;

coupling together a first portion of said first interspersed metal trace to a first portion of said second interspersed metal trace; and

coupling together a second portion of said first interspersed metal trace to a second portion of said second interspersed metal trace.

23. The method of claim 22, wherein said open circuits and coupling is not performed in regions where vias are located.

24. The method of claim 23, wherein said programming is reversible during a subsequent chip revision.

25. The method of claim 21, further comprising removing two vias and inserting two vias at any of a plurality of via layers to thereby program the memory cell.

26. The method of claim 25, wherein said programming is reversible during a subsequent chip revision.

27. The memory cell as in one of claims 24-26, further comprising coupling one of the first and second metal interconnect structures to the first supply potential at a bottom metal layer and coupling the other of the first and second metal interconnect structures to the second supply potential at the bottom metal layer.